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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/709,754 | 05/26/2004 | JOHN M. COHN | BUR920040001US1 | 3753 |

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| EXAMINER | |
|---|---|
| TRIMMINGS, JOHN P | |
| **ART UNIT** | **PAPER NUMBER** |
| 2117 | |
| **MAIL DATE** | **DELIVERY MODE** |
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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/709,754 | COHN ET AL. | |
| | Examiner | Art Unit | |
| | John P. Trimmings | 2117 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *26 May 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) *21-27* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,5,6,9,10,19 and 28-30* is/are rejected.

7)☒ Claim(s) *3-20,28,30* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 May 2007* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

This office action is in response to the applicant's election response dated 8/9/2007.

Claims 1-30 are presented for examination.

### *Election/Restrictions*

1. Claims 21-27 were withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected groups II and III, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 8/9/2007.

### *Drawings*

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character not mentioned in the description: FIG. 3 41.

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, in claim 15, the breakpoint based on a preselected number of clock cycles must be shown or the feature canceled from the claim. The examiner has failed to find any drawing that would suggest that a count of clock cycles and initiation of a breakpoint occurs in the invention. No new matter should be entered.

4. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, in claim 28, "an external in-circuit emulator" and "the in-circuit emulator" must be shown or the features canceled from the claim. The examiner has failed to find any drawing that would suggest that an external in-circuit emulator occurs in the invention. No new matter should be entered.

5. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, in claim 30, the correction of data "in the plurality of scan chains" must be shown or the feature canceled from the claim. The examiner has failed to find any drawing that would suggest that scan chain data correction occurs in the invention. No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate

changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

### *Claim Objections*

6. Claim 28 is objected to because of the following informalities: The examiner requests correction of line 17 to recite, "... repeating the cycling a scan chain data path with ...".

### *Claim Rejections - 35 USC § 112*

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claim 2 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The limitation, "implementing error correction" in line 10 is indefinite because one is not sure if the error correction in the limitation is new, or is the same "error correction ... of a defective logic function" instantiated in the preamble of claim 1, or "error correction for defective data ..." in line 4 above.

9. Claim 5 recites the limitation "the logic function IC" in line 3. There is insufficient antecedent basis for this limitation in the claim.

10. Claims 5 and 6 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The term, "... strategically placed throughout the design ..." is not a positive limitation, and fails to clearly state the metes and bounds of the claim. Further, the examiner has failed to find any further support in the disclosure or the drawings for clearly describing the "strategic" placement of embedded FPGAs, therefore the claim is rejected as being indefinite.

11. Claim 9 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. A broad range or limitation together with a narrow range or limitation that falls within the broad range or limitation (in the same claim) is considered indefinite, since the resulting claim does not clearly set forth the metes and bounds of the patent protection desired. See MPEP § 2173.05(c). Note the explanation given by the Board of Patent Appeals and Interferences in *Ex parte Wu*, 10 USPQ2d 2031, 2033 (Bd. Pat. App. & Inter. 1989), as to where broad language is followed by "such as" and then narrow language. The Board stated that this can render a claim indefinite by raising a question or doubt as to whether the feature introduced by such language is (a)

merely exemplary of the remainder of the claim, and therefore not required, or (b) a required feature of the claims. Note also, for example, the decisions of *Ex parte Steigewald*, 131 USPQ 74 (Bd. App. 1961); *Ex parte Hall*, 83 USPQ 38 (Bd. App. 1948); and *Ex parte Hasche*, 86 USPQ 481 (Bd. App. 1949). In the present instance, claim 9 recites the broad recitation "identifying a plurality of correction solutions", and the claim also recites, "such as correcting bad data bits, correcting upstream data, correcting downstream data ... selecting and implementing one or more of the correction solutions." which is the narrower statement of the range/limitation.

12. Claim 10 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The limitation, "... to enable replacement of a defective logic function." at lines 7 and 8, is indefinite because one does not know if this is a *new instantiation* of "a defective logic function", or if the limitation refers to "a defective logic function of each identified defective logic function".

13. Claim 19 recites the limitation "the scan chain data" in line 2. There is insufficient antecedent basis for this limitation in the claim.

14. Claim 19 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The limitation, "... an incoming scan chain bit stream ..." is

indefinite because one is not sure if the limitation is a new instantiation, or is the same "scan chain data stream" as in claim 18.

15. Claim 30 recites the limitation "the in-circuit emulator" in line 11. There is insufficient antecedent basis for this limitation in the claim.

16. Claim 30 recites the limitation "the logic function repair" in line 17. There is insufficient antecedent basis for this limitation in the claim.

***17.*** Claim 30 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The limitation, "... repair of the embedded FPGA inserted into the scan chain; ..." is indefinite because the examiner cannot find disclosure or drawings that would show an FPGA being inserted into a scan chain in the present application.

***Claim Rejections - 35 USC § 103***

18. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

19. Claims 1, 5, 28, and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bailis et al. (herein Bailis, US Patent No. 6545501.

As per claims 1 and 28:

As best understood in regard to claim 30 in view of the rejections under 35 USC 112 second paragraph, Bailis discloses a method of providing error correction in an integrated circuit (IC) to enable the replacement of a defective logic function implemented within the IC (see Title), the method comprising: providing an embedded field programmable gate array (FPGA) in the IC to perform logic error correction (FIG. 2 124); identifying a defective logic function within the IC (*though not specifically claimed, Bailis presupposes identification of a failure in the logic in the Background*); programming the embedded FPGA to replace the defective logic function (see Title); identifying all inputs in an input cone of logic of the defective logic function (column 3 lines 46-59); directing all inputs in the input cone of logic of the defective logic function into the embedded FPGA (see FIG. 2 input stages into FP 124 and see again column 3 lines 46-59), such that the embedded FPGA replaces the defective logic function with an error corrected version of the defective logic function (see Abstract); identifying all outputs in an output cone of logic of the defective logic function (column 3 lines 46-59); directing an output of the FPGA to the output cone of logic of the defective logic function (see illustration in FIG. 2 where the output stages is programmed at 120'), such that logic error correction is provided within the embedded FPGA structure of the IC (Tiltle). Where Bailis above does not disclose identifying defective logic, the examiner has determined that identifying a defective logic function within the IC is performed by the

Bailis invention, otherwise there would be no process as is described that repairs the failing logic of Bailis. The technique that is claimed by the applicant is a known technique of identifying defective logic (a test result does this) that is applicable to the device, and that one of ordinary skill in the art would have recognized that applying the known technique would have yielded predictable results, and is recognized as part of the ordinary capabilities of one skilled in the art. One of ordinary skill in the art could have pursued the known technique in the applicant's invention with a reasonable expectation of success, and so the claim is rejected.

As per claims 5 and 29:

Bailis further discloses the method of claim 1, wherein a plurality of said embedded FPGAs are strategically placed throughout the design of the logic function IC. FIG. 2 illustrates the placement of the FPGAs in proximity to all logic blocks. And in view of the rationale above, the claims are rejected.

***Allowable Subject Matter***

20. Claims 3-20 and 30 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims, and any outstanding rejections under 35 USC 112 second paragraph are corrected. The following is a statement of reasons for the indication of allowable subject matter: The reference Bailis teaches a method of correcting failures in logic elements of an IC containing also FPGA logic that replaces faulty logic elements based on determining a failing element and subsequent

input/output connections by a trial and error process. But the reference has failed to further teach, suggest or disclose the unique features as claimed by the applicant in claims 3-20 and 30, wherein the replacement and programming of the replacement logic is performed through a scan chain input and output of the IC that defines a data path through the IC.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John P. Trimmings whose telephone number is (571) 272-3830. The examiner can normally be reached on Monday through Thursday, 7:00 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques Louis-Jacques can be reached on (571) 272-6962. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/John P Trimmings/
Examiner, Art Unit 2117
8/14/2007

jpt